Ronny Abdullah

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Education & Relevant Coursework

Stanford University **Stanford, CA**

*B.S. in **Electrical Engineering**, GPA: 3.5* *Sept. 2022 – June 2026*

*M.S. in **Electrical Engineering**, GPA: 4.0* *June 2026 – June 2027*

- **VLSI & Microarchitecture:** Introduction to VLSI Systems, VLSI Design Projects, Digital Systems Engineering
- **Computer Architecture & Systems:** Digital System Design, Digital Systems Architecture, Operating Systems
- **Embedded & Circuits:** Embedded Systems, Board-Level Design, Circuits I & II, Autonomous Implantable Systems
- **Math & Foundations:** Signals & Systems, Probability, Data Structures & Algorithms, Continuous Math Methods

Experience

Stanford Robust Systems Group (Prof. Subhasish Mitra) **September 2024 – Present**

Researcher – RTL Design & Hardware Verification *Stanford, CA*

- Designed **7** SystemVerilog RTL modules for accelerator datapaths (MAC control, SRAM scheduling, ready/valid interfaces).
- Authored **45+** SVA and **120+** directed/constrained-random tests, uncovering **6** corner cases including deadlock and illegal handshakes.
- Built nightly regressions across **2,000+** simulation seeds, raising functional coverage from **62%** to **91%**.

Teaching Assistant – ENGR 40M; EE 101A **March 2025 – June 2026**

Stanford University *Stanford, CA*

- Led weekly lab sections/quarter (**20–25** students each) on digital logic, circuit analysis, PCB bring-up, and firmware.
- Ran **15+** debugging sessions/quarter on board bring-up failures and firmware bugs (interrupts, timers, peripherals).
- Rewrote starter code and validation tests to eliminate the most common board bring-up failures.

XDR Radiology **June 2025 – September 2025**

Software Engineering Intern – Backend Systems *Los Angeles, CA (Hybrid)*

- Built **5+** backend services and **12+** REST endpoints for study ingestion and workflow state management.

Projects

SIMD Matrix-Multiply Accelerator **SystemVerilog, Catapult HLS (SystemC), Synopsys DC**

Introduction to VLSI Systems / VLSI Design Projects

- Designed a SIMD accelerator with PE datapath, controller FSM, and on-chip memory buffer for matrix-multiply workloads.
- Optimized RTL via multiplier reuse, retiming, clock gating, and PE scaling, hitting **FoM $<$ 50** within **1 mm^2**.
- Closed timing in Synopsys DC via critical-path analysis, pipeline-stage insertion, and iterative synthesis.

5-Stage Pipelined MIPS Processor **SystemVerilog, Xilinx Zynq FPGA**

Digital Systems Architecture

- Implemented a 5-stage pipelined MIPS core with **40+** ops (ALU, load/store, branches, LL/SC) at single-cycle throughput.
- Designed RAW-hazard detection, data forwarding, branch delay-slot handling, and precise stall control.

Wave-Table Music Synthesizer (FPGA) **Verilog, Digital System Design**

Digital System Design

- Built an FSM-driven wave-table synthesizer using ROM lookup tables to generate sine-wave audio with sequencing control.
- Designed a real-time VGA audio-visualization datapath with double-buffering to render clean waveforms.

Gesture-Controlled RC Car with Live Camera Streaming **C, STM32 (ARM Cortex-M)**

Embedded Systems

- Wrote bare-metal C firmware configuring UART, PWM timers, and SPI/I^{2}C for a Bluetooth-controlled car with live camera streaming.
- Debugged real-time timing faults using logic-analyzer traces to validate peripheral and control timing.

FM Stereo Radio Receiver **Board Bring-Up, RF Signal Chain, PCB Rework**

Board-Level Design

- Populated and brought up a multi-component FM receiver PCB (RDA5807 front-end, LDO regulation, RF passives, SMD + through-hole).
- Debugged connectivity and solder bridges via DMM continuity and microscope inspection; verified tuning and voltage regulation.

Technical Skills

RTL & Verification: SystemVerilog, Verilog, SVA, constrained-random/directed testbenches, functional coverage, FSM design, pipelining, timing closure, clock gating
Tools / Flow: Synopsys Design Compiler, Xilinx Vivado, FPGA (Xilinx Zynq), Git, Linux, Docker, TCL
Programming: C, C++, Python, x86-64 Assembly, ARM Assembly, JavaScript
Embedded & Hardware: STM32 (ARM Cortex-M), GPIO, Timers, Interrupts, DMA, ADC/DAC, UART, SPI, I^{2}C, PCB Design

Leadership / Extracurricular

Stanford Moonshot Club **September 2022 – Present**

Undergraduate Member *Stanford, CA*

- Engineered a motorized couch with embedded control systems, reaching **2.5M+ views** and **300K+ likes** online.